semiconductor device comprising plural adjacent transistor cells provided with a gate electrode and a diffusion layer disposed adjacent to each of opposite end portions of said gate electrode, the method comprising the steps of:

forming a conductive layer on a semiconductor substrate through an insulation film;

patterning said conductive layer to form said gate electrode together with a shielding electrode, wherein said shielding electrode is disposed adjacent to each of opposite end portions of said gate electrode to extend in parallel with said gate electrode;

injecting an impurity into said semiconductor substrate in a self-align manner with the use of both said gate electrode and said shielding electrode as masks to form said diffusion layer; and

insulating said gate electrode in each of said transistor cells,

wherein said diffusion layer forms a diffusion line extending, in a completed device, between said adjacent transistor cells.--

Amend claim 2 as follows:

--2. (amended) In a method of manufacturing a nonvolatile semiconductor memory device provided with a plurality of integrated nonvolatile semiconductor memory cells each comprising: a lower floating gate; a control gate formed on said

lower floating gate through an insulation film; a diffusion layer disposed adjacent to each of opposite end portions of said lower floating gate, the method comprising the steps of:

forming a first conductive layer on a semiconductor substrate through an insulation film;

patterning said first conductive layer to form said lower floating gate together with a device isolation shielding electrode, wherein said shielding electrode is disposed adjacent to each of opposite end portions of said gate electrode to extend in parallel with said lower floating gate between plural of said nonvolatile memory cells in a completed device; and

injecting an impurity into said semiconductor substrate in a self-align manner with the use of both said lower floating gate and said device isolation shielding electrode as masks to form said diffusion layer,

wherein said diffusion layer forms a diffusion line extending, in the completed device, between adjacent ones of said nonvolatile memory cells.--

Add the following new claim:

--10. (new) In a method of manufacturing a semiconductor device provided with a gate electrode and a diffusion layer disposed adjacent to each of opposite end portions of said gate electrode, the method comprising the steps of:

forming a conductive layer on a semiconductor substrate

through an insulation film;

patterning said conductive layer to form said gate electrode together with a shielding electrode, wherein said shielding electrode is disposed adjacent to each of opposite end portions of said gate electrode to extend in parallel with said gate electrode;

injecting an impurity into said semiconductor substrate in a self-align manner with the use of both said gate electrode and said shielding electrode as masks to form said diffusion layer covering adjacent ones of transistor cells; and

insulating said gate electrode in each of said transistor cells,

wherein said diffusion layer of each of said transistor cells are of the same width and form diffusion lines extending, in a completed device, between adjacent memory cells.--

REMARKS

The application has been amended so as to place it in condition for allowance at the time of the next Official Action.

The specification has been amended as to form.

Claims 1-10 are pending with claims 1-2 and new claim 10 being independent.

The Official Action rejected claims 1-7 under §102 as anticipated by BERGEMONT 5,847,426.

The Official Action rejected claims 8-9 under §103 as obvious over BERGEMONT in view of SAITOH 5,985,720.